REMARKS

This is in response to the Office Action mailed June 25, 2004. Applicant respectfully traverse and request reconsideration.

Rejection of claims under 35 U.S.C. § 102

Claims 1, 3 through 4, 9 through 12 and 16 currently stand rejected under 35 U.S.C. § 102(b) based on U.S. Patent No. 6,243,817 ("Melo"). Applicant submits the present rejection is improper because Melo fails to disclose all of the claimed limitations.

Melo

Melo is directed to a device (a computer) and method for dynamically reducing power consumption within input buffers of a bus interface unit. (Melo, title.) Throughout the specification Melo describes the invention relating to a computer. (Melo, abstract, col. 1, line 9; col. 3, lines 6—7, col. 4, line 41; col. 6, lines 6—12; col. 6, line 56.) Melo seeks to solve the problem of reducing power consumption in a portable computer having a bus that employs differential signals to help extend the battery life of the computer. (Melo col. 2, lines 24—26) Hence, Melo seeks to solve these problems in an improved power management technique in a computer. (Melo col. 2, lines 29—30; col. 2, lines 24—26.) The AGP (Accelerated Graphics Port) is physically, logically and electrically independent of the PCI bus and intended for the exclusive use of a display device 22 coupled to the graphics port (or AGP) by a graphics accelerator 20 and local memory or frame buffer 24. (Melo col. 4, lines 63—67) North bridge 14 is generally considered an application specific chip set, or application specific integrated circuit (ASIC) that provides connectivity to various buses and integrates other system functions such as memory interface and P 1394. (Melo col. 5, lines 10-14) Similar to north bridge 14, south bridge 28 is an ASIC or group of ASICs that provides connectivity between various buses and may also include system functions that can possibly integrate one or more serial ports. (Melo col. 5, lines 23—26.)

According to the Office Action on page 2, "in regard to claims 1, 10 and 12 in FIG. 2, Melo discloses an IC comprising: *a standard dimension substrate, not shown*, where the components disposed thereon . . . ." (Emphasis added.)

Claims 1 and 10

Claim 1 recites:

To anticipate a claim the Office Action must show where the cited reference teaches each and every element as arranged in the claim.

1. An integrated circuit comprising:

a standard dimension carrier substrate;

an information router integrated on the carrier substrate; and

system memory operative to store system instructions also integrated on the carrier substrate and in electrical communication with the information router via at least one of a plurality of electrical leads associated with the carrier substrate, wherein the system instructions may be stored and retrieved from the system memory through the information router.

As acknowledged in the Office Action on page 2, reference no. 2, FIG. 2 does not show "a standard dimension carrier substrate." According to Melo, FIG. 2 describes a computer that comprises a power management device that can turn off various clocks of the computer subcomponents in order to save power. (Melo col. 6 lines 6—9.) The Office Action does not attempt to explain how Melo otherwise teaches "a standard dimension carrier substrate." As a result, and as acknowledged in the Office Action, Melo fails to show "a standard dimension substrate." Therefore, the Office Action fails to show how Melo describes each and every element as arranged in the claims. The Applicant requests a showing per 37 CFR 1.104(c)(2) of where Melo describes "a standard dimension substrate."

Further, Melo appears to be directed to a computer. (Melo col. 4, line 41; col. 6, lines 6—11, line 56, etc.) Melo, therefore, rather than teaching a "standard dimension substrate," is directed instead to a computer.

Regarding claim 2, the Office Action cites to FIG. 1 to teach "an application specific die." However, FIG. 1 merely shows a block diagram of a processor and other components, rather than, "an application specific die." Accordingly, the Applicant requests a showing of "an application specific die" in Melo, as cited.

Regarding claim 3, the Office Action asserts that Melo in FIG. 1, discloses "a graphics controller 20 disposed within the application specific IC die." However, as previously stated, FIG. 1 illustrates a processor and other components, rather than, "an application specific die." Further, Melo teaches "AGP is physically, logically, and electrically independent of the PCI bus and intended for the exclusive use of a display device 22 coupled to the graphics port (or AGP) by a graphics accelerator 20 and local memory or frame buffer 24." (Col. 4, lines 63—67.) Since Melo teaches that the AGP is physically as well as logically and electrically independent of the PCI bus, Melo teaches away from "a standard dimension substrate." The Office Action, therefore, misinterprets Melo and ignores a principal element in the claims, namely "a standard dimension substrate." Applicants requests a showing per 37 CFR 1.104(c)(2) of where Melo, as cited, teaches "a graphics controller further disposed within the application specific die in conjunction with the information router."

Regarding claims 9 and 16, the Applicant repeats the above relevant remarks. Further, the Office Action merely cites to FIG. 1, which shows a block diagram of a processor and other components, rather than, "wherein the information router within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board." The Office Action fails to show where Melo describes a printed circuit board let alone "wherein the information router within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board." Therefore, the Applicant requests a showing of "wherein the information router within the application specific integrated circuit die is capable of being operably coupled to a central

processing unit across a printed circuit board." As a result, the Office Action fails to show where Melo teaches each and every element as arranged in the claims.

Regarding claim 11, the Applicant repeats the above relevant remarks. Further, the Office Action merely cites to FIG. 1, which shows a block diagram of a processor and other components, rather than "wherein the application specific integrated circuit die further includes a graphics controller in conjunction with the north bridge." The Applicant requests a showing of where Melo teaches "wherein the application specific integrated circuit die further includes a graphics controller in conjunction with the north bridge."

Dependant claims 3, 4 and 9 depend from claim 1, and claims 11 and 16 depend from claim 10 and contain further novel and nonobvious subject matter not contained in the independent claims. Therefore, reconsideration and withdrawal of the present rejections is respectfully requested.

Rejection of claims under 35 U.S.C. § 103(a)

Claims 5 through 8 and 13 through 15 are rejected under 35 U.S.C. § 103(a) based on Jeddeloh (United States Patent No. 6,346,446) as applied to claims 1, 3 through 4, 9 through 12, and 16 above and further in view of U.S. Patent Application No. 2003/0183934 ("Barrett"). However, the Office Action applied Melo to claims 1, 3 through 4, 9 through 12 and not Jeddeloh. Although the Office Action makes reference to the Jeddeloh reference that was previously cited in the previous office action, the Applicant will address both references in this rejection in the event the primary reference was intended to be Melo.

Melo

According to the Office Action in regards to claims 5—8 and 13—15, Melo fails to disclose "a die coupled to the bottom using wirebonds and flip chip technology." Further, the Office Action states on page 4, lines 5 through 8, with regards to Barrett, "the package is put together by using wirebond and flip chip technology in order to reduce the package size and costs when more than one die is needed; see [0010]." However, paragraph 10 of Barrett states:

> FIG. 3 is a block diagram of one embodiment of a package with a die 350 mounted to a surface of another die 310 which is then mounted to a substrate 330. This differs from prior flip chip packages such as that shown in FIG. 2 in that one die is mounted to another die rather than mounting each die adjacent to each other on substrate. The configuration of FIG. 3 results in a reduction of package size and cost when more than one die is needed.

The combination of Melo and Barrett teaches a computer, die 350, and die 330 on a die 310 with a flip chip package. Rather than teach wirebonds, the cited portion of Barrett and also the combination of Melo and Barrett does not describe "wherein the application specific integrated circuit die is coupled to at least one of the plurality of electrical leads associated with the carrier substrate using a plurality of wirebonds." The undersigned cannot find where the cited portions of Barrett nor Melo teach "wirebonds" let alone each and every element as arranged in claim 5, including "wherein the application specific integrated circuit die is coupled to at least one of the plurality of electrical leads associated with the carrier substrate using a plurality of wirebonds." As a result, the Office Action fails to show where the combination of the Barrett and Melo, to the extent that these two references can be combined, describes each and every limitation as arranged in the claims including "a wirebond." The Applicant requests a showing of where Barrett, as cited, teaches "wherein the application specific integrated circuit die is coupled to at least one of the plurality of electrical leads associated with the carrier substrate using a plurality of wirebonds."

Jeddeloh

In support of the previous rejection, the Examiner has indicated that the claimed system memory of the present invention is disclosed by Jeddeloh as the processor interface 126. Applicants respectfully disagree and submit that the processor interface 126 of Jeddeloh is what it is described to be: an interface including circuitry for communicating with processors attached to a processor bus 108. (*See* col. 4, lines 21—23. As noted above, during the telephone interview with the Examiner, the Examiner indicated that the processor interface 126 would inherently contain memory that discloses the system memory, with which Applicant disagrees.

Applicant respectfully submits that the Examiner has improperly interpreted the term interface with respect to the processor interface 126 of Jeddeloh. The Examiner's interpretation is not only beyond the plain and ordinary meaning of the term interface as defined by the specification of Jeddeloh, which is silent as to a specific definition of a processor interface other than its ordinary meaning. For example, as used in column 3, lines 23—24 Jeddeloh states, "processor interface 126 for communicating with processor bus 108." Furthermore, the Examiner has provided an interpretation beyond the meaning of the term interface. While Applicant appreciates the Examiner's broad interpretation of the interface inherently containing memory, Applicant submits that the Examiner is improper in asserting this as disclosing the claimed limitation of system memory as claimed in claims 1 and 10. Claims 1 and 10 recite the system memory operative to store system instructions wherein the system instructions may be stored and retrieved from the system memory.

Even assuming, *arguendo*, that the interface 126 of Jeddeloh does include some type of temporary memory for interfacing, this would not constitute the claimed system memory of claims 1 and 10 and it is not operative to store system instructions but is only operative to store transient data in an interface setting, which is inconsistent with the claimed present invention. More specifically, the system of Jeddeloh operates in a completely different manner, which is providing a specific interface between the north bridge 102 and processor 112—116 across the processor bus 108, and produces a completely different result, which is having system memory located outside of the north bridge, which would require further processing delay for getting information across the processor bus. In other words, Jeddeloh describes specifically the prior art approach that the present invention overcomes because, among other things, the processor interface does not contain the claimed system memory of the present invention but only provides for interfacing with the processors 112—116 across the processor bus 108 for access through the switch 124 as described in the corresponding specification of Jeddeloh.

Therefore, Applicant respectfully requests reconsideration and withdrawal of the present rejection. Should the Examiner maintain the present rejection, Applicant requests a showing per 37 C.F.R. §1.104(c)(2), including specific column and line numbers, of the exact delineation of where the processor interface 126 of Jeddeloh discloses including memory constituting the

system memory, as claimed in the present invention. In the alternative, Applicant requests further support of the Examiner's position of the inherency of memory within the processor interface 126 and support for the inherent memory to constitute the claimed system memory of the present invention.

Regarding claims 2 through 4, 9 and 11 through 12, Applicant respectfully resubmits the above position offered with regards to claims 1 and 10, respectively, and submits that these claims contain further patentable subject limitations therein. It is further submitted these claims are allowable not merely as being dependent upon an allowable base claim, but also because Jeddeloh fails to disclose all of the claimed limitations, including, but not limited to, the system memory disposed within the integrated circuit of the present invention. Therefore, reconsideration and withdrawal of the present rejection is respectfully requested.

According to the Office Action, "in regard to claim 2 the router is disposed within an application specific die; see FIG. 1." However, the Office Action fails to show where in FIG. 1 an application specific die is shown. Further, the Office Action fails to show where a router is shown, let alone "wherein the information router is disposed within an application specific integrated circuit die." Accordingly, the Applicant respectfully requests the Examiner to specifically show where Melo in FIG. 1 describes "wherein the information router is disposed within an application specific integrated circuit die." The Applicant repeats the above remarks with regard to at least claim 1. Applicant respectfully requests that the Examiner show pursuant to 37 C.F.R. §1.104(c)(2) where in FIG. 1 Melo describes "an application specific die."

Regarding claims 5 through 8 and 13 through 16, Applicant respectfully resubmits the above position offered with regard to claims 1 and 10, respectively, and submits these claims contain further limitations therein. It is further submitted these claims contain patentable subject matter and are allowable not merely as being dependent upon an allowable base claim, but also because the combination of Jeddeloh, Melo or Barrett fails to teach or suggest, among other things, the claimed system memory disposed within the integrated circuit of the present invention. Therefore, reconsideration and withdrawal is respectfully requested.

Accordingly, Applicant respectfully submits that the claims are in condition for allowance and request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: August 25, 2004

By: _____
Themi Anagnos
Registration No. 47,388

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ, P.C.
222 North LaSalle Street
Chicago, IL 60601
Telephone: (312) 609-7870
Facsimile: (312) 609-5005
Email: tanagnos@vedderprice.com